REMARKS/ARGUMENTS

**Present Status of Application**

Claims 1-6 and 11-16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa (U.S. 5,308,682).

Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa (U.S. 5,308,682) in view of Ziger (U.S. 6,327,513).

Claims 8, 10 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa (U.S. 5,308,682) in view of Ziger (U.S. 6,327,513)and in further view of Suzuki et al (U.S. 5,189,707).

**Insufficiency of the rejections**

The Examiner thanks Applicant for being in a spirit of cooperation in trying to understand the Examiner's rejections. Unfortunately, the Examiner does not show the Applicant the same level of cooperation nor does the Examiner comply with the rules of practice.

If the Examiner forces the Applicant to take this matter on appeal, then the Applicant with request a pre-appeal conference and will demand full compliance with the rules of practice at that time if the Examiner continues to fail to fully comply with the rules of practice.

In rejecting Claims 1-6, 11-16 and 20, the Examiner tries to read the said first, second, third and fourth checking patterns on all 19 Figures of Morikawa. What the Examiner does is point the Applicant to all of the Figures in the cited reference and apparently expects the Applicant to try to figure out which shapes or patterns among the 19 Figures comprise the patterns recited in Claim 1, for example.

With all due respect to the Examiner, that is a flagrant violation of the Rules of Practice.

The Applicant politely responded in the first Official Action and requested the Examiner to point out exactly how the claims were anticipated by the prior art reference. In the spirit of cooperation, the Applicant amended the claims in a way that it was hoped would clearly overcome the reference based upon the Applicant's assumptions of how the Examiner was reading what on what. Obviously, the Applicant's assumptions were wrong since the Examiner continues to reject the claims in this Application. However, the Examiner still refuses to point out with specificity just how the limitations of each and every rejected claim noted above can be read upon this prior art reference.

For example, claim 1 recites, *inter alia*, "forming a first checking pattern on a first semiconductor layer", exactly where is that shown in the cited reference? Please answer the same question for the recited "second checking pattern on a second semiconductor layer" third checking pattern on a third semiconductor layer" and "fourth checking pattern on a fourth semiconductor layer".

Claim 1 also recites, *inter alia*, "the first, second and third checking patterns in their entireties overlap to form a first rectangular frame", exactly where is that shown in the cited reference?

Claim 1 also recites, *inter alia*, "the fourth checking pattern in its entirety is surrounded by the first rectangular frame," exactly where is that shown in the cited reference?

Claim 1 further recites, *inter alia*, "a first pair of parallel sides of the first rectangular frame is formed by the first checking pattern, and a second pair of parallel sides of the first rectangular frame is formed by the second and third checking patterns", exactly where is that shown in the cited reference?

Claim 1 also recites, *inter alia*, " measuring overlap accuracy between the fourth checking pattern and the first checking pattern; and measuring overlap accuracy between the fourth checking pattern and the second and third checking patterns", exactly where is that shown in the cited reference?

Interestingly, the Examiner seems to agree that Morikawa fails to anticipate independent claims 1 and 11 since the Examiner states in the official action "Morikawa may not teach the exact claimed shape." Since claim 1 does not use the word "shape" just what shape in Morikawa (or the claims) is the Examiner referring to? Is it the claimed "rectangular frame"? Well, first the Examiner has the obligation under the rules of practice to spell out exactly where Morikawa teaches "a first ... frame" as recited by both claims 1 and 11. Based on the Examiner's comment, the reader is lead to believe that whatever "first frame" the Examiner has in mind must have a non-rectangular shape given the Examiner's comment about changing it's shape. So exactly what non-rectangular first frame in Morikawa is the Examiner referring to? Only after that has been clarified can the issue of whether or not there is any motivation in

the art to modify Morikawa's first frame (whatever that might be) to have a rectangular shape. Exactly what problem to being addressed by modifying Morikawa? If nothing in Morikawa needs to be "fixed" there where is the motivation to modify Morikawa coming from? Based on the information supplied by the Examiner to date, it seems that the motivation is coming from one place: applicant's claims. That is an improper use of applicant's own disclosure against applicant!

Since the Examiner has not pointed out how each and every limitation of the Claims can be found in the prior art reference or when there is motivation in the prior art to alter the prior art reference, the rejection is utterly improper.

The same problems arise in the Examiner's rejection of the rejected dependent claims note above.

The same issues also arise in the Examiner's rejection of claims 7, 8, 10, and 17-19. Since the Examiner has not spelled out what portions of Morikawa are relevant to the claims pending in this application it is next to impossible to analyze the Examiner's comments with respect to why it he thinks be obvious to try to combine Morikawa with Ziger and/or Suzuki. Exactly what deficiencies in Morikawa does the Examiner believed are overcome by these secondary references?

The Examiner's rejections based on Ziger, for example, are also very unclear. The Examiner refers to "subtracted locations" in Ziger. Since Ziger does not use the term "subtracted locations" exactly what is the Examiner referring to? It is not the applicant's job to have to figure out what is on the Examiner's mind when making a rejection. But it is the Examiner's obligation, under the rules of

practice, to make the rejection clear and to point out with specificity what the Examiner is referring to.

Moreover, the Applicant respectfully submits that the rejections are also insufficient, insofar as they do not comply with the requirements of MPEP 707.07 et seq., which require that all rejections be stated with completeness and clarity. More specifically, MPEP 707.07(d) requires that the grounds for rejection for rejection be "fully and clearly stated." The Office Action has failed to do this in the present application.

Indeed, in rejecting Claims 1-6, 11-16 and 20, the Examiner tries to read into said first, second and third checking patterns onto all 19 figures of Morikawa. What the Examiner does is point the Applicant to all of the figures in the cited reference and apparently expects the Applicant to try to figure out which patterns among the 19 figures comprises the patterns to which the Examiner makes reference and how those patterns.

With all due respect to the Examiner, that is a clear violation of the Rules of Practice.

The Applicant politely responded in the first Official Action and requested the Examiner to point out exactly how the claims were anticipated by the prior art reference. In the spirit of cooperation, the Applicant amended the claims in a way that it was hoped would clearly overcome the reference based upon the Applicant's assumptions of how the Examiner was reading what on what. Obviously, the Applicant's assumptions were wrong since the Examiner continues to reject the claims in this Application. However, the Examiner still fails to point out with specificity just how the limitations pending in this Application read upon this prior art reference.

That is improper and, if need be, the Applicant will request an Appeal Brief Conference in which the Examiner will be required to comply with the Rules of Practice.

Since the Examiner has not pointed out how each and every limitation of the Claims can be found in the prior art reference, the rejection is utterly improper.

**Additional comments on the rejections and Examiner assertions**

**1. Rejections Under 35 U.S.C. 103(a) of Claims 1-6 and 11-16 and 20**

Claims 1-6 and 11-16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa (U.S. 5,308,682). Applicant asserts that claim 1 is patentable for the reasons discussed below.

The examiner asserts that "Applicant's arguments filed on 1/3/06 have been fully considered but they are not persuasive. Applicant has amended claims 1 and 11 to include the phrase "in their entireties" and "in their entirety". **Examiner asserts that "Moikawa discloses checking patterns that are surrounded by their checking patterns in its entirety (figure 5b, item 34, which is a second checking pattern, is enclosed entirely in item 33w1, which is a first checking pattern.** Therefore, Examiner believes that this teaches Applicants amendment to claims 1 and 11".

Applicant, however, does not agree with this assertion.

**Claim 1 recites:**

1. A method of checking overlap accuracy of patterns on

four stacked semiconductor layers, comprising:

forming a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns **in their entireties overlap to form *a first rectangular frame***, the fourth checking pattern in its entirety is surrounded by the first rectangular frame, a first pair of parallel sides of the first rectangular frame is formed by the first checking pattern, and a second pair of parallel sides of the first rectangular frame is formed by the second and third checking patterns;

measuring overlap accuracy between the fourth checking pattern and the first checking pattern; and

measuring overlap accuracy between the fourth checking pattern and the second and third checking patterns. (Emphasis Added)

It is clear that the method of checking overlap accuracy of patterns on four stacked semiconductor layers of claim 1 comprises **the first, second and third checking patterns in their entireties overlapping to form a first rectangular frame**.

The Examiner asserts that in figure 5b Morikawa discloses that the item 34, which is characterized by the Examiner as a second checking pattern, is enclosed entirely in item 33w1, which is characterized by the Examiner as a first checking pattern.

However, referring to Col. 5, line 66 to Col. 6, line 34 and FIG. 5a and 5b, Morikawa teaches:

> "As shown in FIG. 5a, ***first level wirings 33W1 and 33W2 are formed on a surface of the insulating film 32 over a substrate at a wiring forming region.*** The regular scale patterns 23a-23e of the first alignment check pattern shown in FIG. 2a, the dummy patterns 35a-35d of the second alignment check pattern shown in FIG. 3b and the first dummy patterns 33a-33d of the third alignment check patterns shown in FIG. 3d are also formed simultaneously with the first-level-wiring formation. After sputtering an aluminum film on the insulating film 32 and patterning the aluminum film, those wirings and patterns are formed. Each of the wirings 33W1 and 33W2, and the patterns 23a-23e, 35a-35d and 33a-33d is made of the same aluminum film, and have same thickness.
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> "As shown in FIG. 5b, the first interlayer insulating film 34, which covers the first level wirings, the regular scale pattern of the first alignment check pattern, the dummy pattern of the second alignment check pattern, the first dummy pattern of the third alignment check pattern and the insulating film 32, is formed. On the first interlayer insulating film 34, a photoresist film 39 is formed. ***In addition, openings 301 and 302, which are for through hole formation, are provided for the film 39.*** In the figure, the underlying insulating film 34 appears at the openings 301 and 302. vernier scale patterns of the first alignment check pattern are also formed at the same time when the openings are formed. An alignment check, which uses the regular scale patterns and the vernier scale patterns of the first alignment check pattern, is performed. After the alignment check, first through holes 303 and 304 are provided for the first interlayer insulating film 34 using the photoresist film 39 as an etching mask. As the vernier scale patterns 25a-25e are openings provided for the photoresist film 39, openings are formed at the first-alignment-check-pattern part of the first interlayer insulating film 34." (Emphasis added)

It is clear that the Examiner's analysis is, with all due respect, unfair. Morikawa indeed teaches the first interlayer insulating film 34 (unfairly characterized by the Examiner as a second checking pattern) formed on a first level wiring 33W1

(unfairly characterized by the Examiner as a first checking pattern), wherein the first interlayer insulating film 34 comprises an opening 301 aligned to the first level wiring 33W1.

The portion of Morikawa reproduced above does mention alignment check patterns, but the Examiner does not refer to them in making this rejection. So exactly why would anyone skilled in this art consider an "interlayer insulating film 34" to really be a "second checking pattern" as claimed? Why would anyone skilled in this art consider an "first level wirings 33W1" to really be a "first checking pattern" as claimed, especially when Morikawa specifically mentions first and second "alignment check patterns"? With all due respect, the Examiner is just pointing to patterns shown in Morikawa's drawings with no regard being given to that which Morikawa really teaches.

MPEP 2142 reads in part:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

> To establish prima facie obviousness of a claimed invention, **all the claim limitations must be taught or suggested by the prior art**. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F. 2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Applicant submits that Morikawa fails to teach or suggest all of the limitations recited in Claim 1. Indeed, the first level wiring 33W1 and the interlayer insulating film 34 in Morikawa do not meet any the first and second checking patterns as recited by Vlaim 1, nor has the examiner pointed out how the remaining portions of Claim 1 are allegedly met by Morikawa..

For at least this reason, it is Applicant's belief that Claim 1 is allowable over the cited reference. Reconsideration of this rejection is hereby respectfully requested.

**Claim 11 recites:**

> 11. A method of checking overlap accuracy of patterns on four stacked semiconductor layers, comprising:
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> forming a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein ***the first, second and third checking patterns in their entireties overlap to form a first rectangular frame***, a first pair of parallel sides of the first rectangular frame is formed by the first checking pattern, a second pair of parallel

sides of the first rectangular frame is formed by the second and third checking patterns, and the fourth checking pattern in its entirety is arrayed as a second rectangular frame and is surrounded by the first rectangular frame;

measuring overlap accuracy between the fourth checking pattern and the first checking pattern; and

measuring overlap accuracy between the fourth checking pattern and the second and third checking patterns. (Emphasis Added)

It is clear that the method of checking overlap accuracy of patterns on four stacked semiconductor layers of claim 11 comprises ***the first, second and third checking patterns in their entireties overlapping to form a first rectangular frame.***

It is not understood how this limitation is in any way met or suggested by Morikawa's disclosure of either a first level wiring 33W1 and/or an interlayer insulating film 34.

For the reasons already described, it is respectfully Morikawa also fails to teach or suggest all of the limitations recited in Claim 11. It is Applicant's belief that Claim 11 is allowable over the cited reference. Reconsideration of this rejection is hereby respectfully requested.

Reconsideration is requested along with withdrawal of the rejections and allowance of the claims.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

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(Date of Transmission)

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May 30, 2006
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